SDLS161

SN54LS348, SN74LS348 (TIM9908)
8-LINE TO 3-LINE PRIORITY ENCODERS
WITH 3-STATE OUTPUTS
OCTOBER 1976 — REVISED MARCH 1988

- **3-State Outputs Drive Bus Lines Directly**
- **Encodes 8 Data Lines to 3-Line Binary (Octal)**
- **Applications Include:**
  N-Bit Encoding
  Code Converters and Generators
- **Typical Data Delay . . . 15 ns**
- **Typical Power Dissipation . . . 60 mW**

description

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The 'LS348 circuits encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion. Outputs A0, A1, and A2 are implemented in three-state logic for easy expansion up to 64 lines without the need for external circuitry. See Typical Application Data.
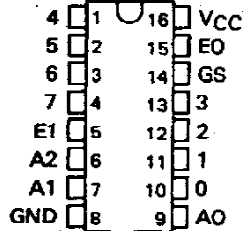
SN54LS348 . . . J OR W PACKAGE
SN74LS348 . . . D OR N PACKAGE
(TOP VIEW)

```
         ___ ___
   4 [ 1 U 16 ] VCC
   5 [ 2    15 ] EO
   6 [ 3    14 ] GS
   7 [ 4    13 ] 3
  E1 [ 5    12 ] 2
  A2 [ 6    11 ] 1
  A1 [ 7    10 ] 0
 GND [ 8     9 ] A0
```

SN54LS348 . . . FK PACKAGE
(TOP VIEW)

```
          5  4  NC VCC EO
          3  2  1  20 19
   6 [ 4            18 ] GS
   7 [ 5            17 ] 3
  NC [ 6            16 ] NC
  E1 [ 7            15 ] 2
  A2 [ 8            14 ] 1
          9 10 11 12 13
          A1 GND NC A0 0
```

NC — No internal connection

logic symbol†

FUNCTION TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	Z	Z	Z	H	H
L	H	H	H	H	H	H	H	H	Z	Z	Z	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

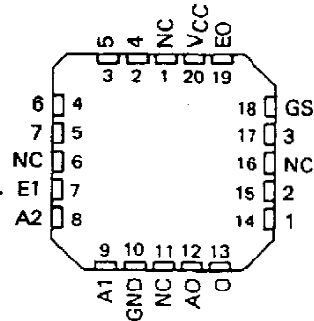H = high logic level, L = low logic level, X = irrelevant
Z = high-impedance state

logic symbol†

```
                    HPRI/BIN
                      ▷
0 (10) ─────────┤ 0/Z10      10 ┤ ≥1
1 (11) ─────────┤ 1/Z11      11 ┤
2 (12) ─────────┤ 2/Z12      12 ┤
3 (13) ─────────┤ 3/Z13      13 ┤
4 (1)  ─────────┤ 4/Z14      14 ┤        (15)
5 (2)  ─────────┤ 5/Z15      15 ┤   18 ──── EO
6 (3)  ─────────┤ 6/Z16      16 ┤  19ENα  (14)
7 (4)  ─────────┤ 7/Z17      17 ┤    ──── GS

                                   1α ▽ (9) ── A0
            V18                    2α ▽ (7) ── A1
EI (5) ─────── G19                 4α ▽ (6) ── A2
```

†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
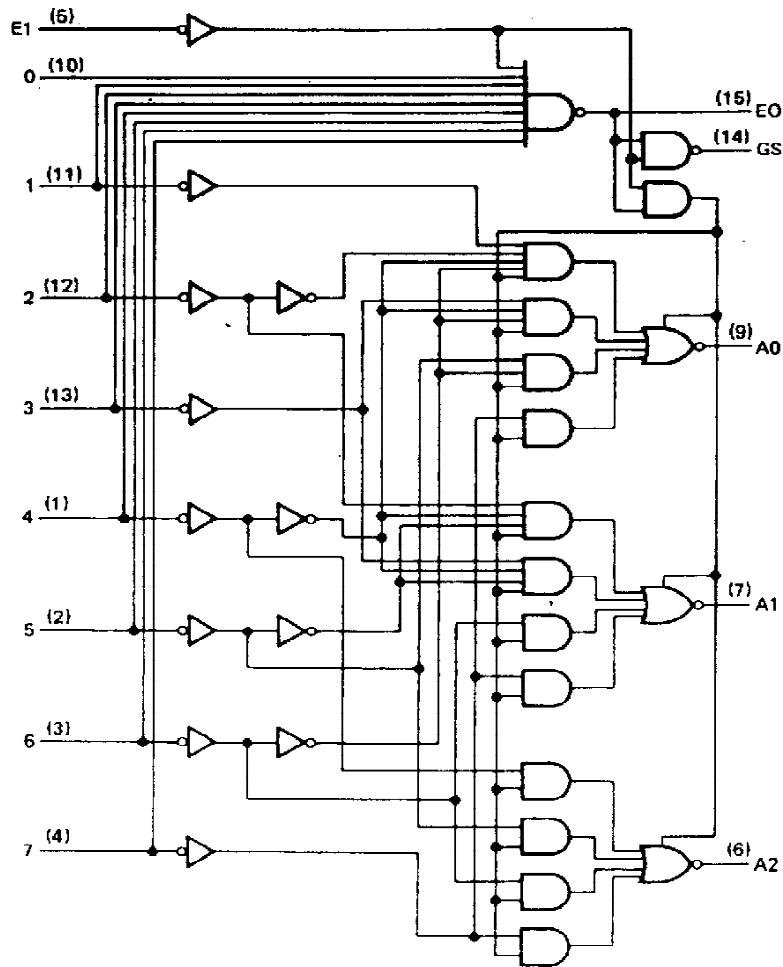Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

Pin numbers shown are for D, J, N, and W packages.

schematic of inputs and outputs
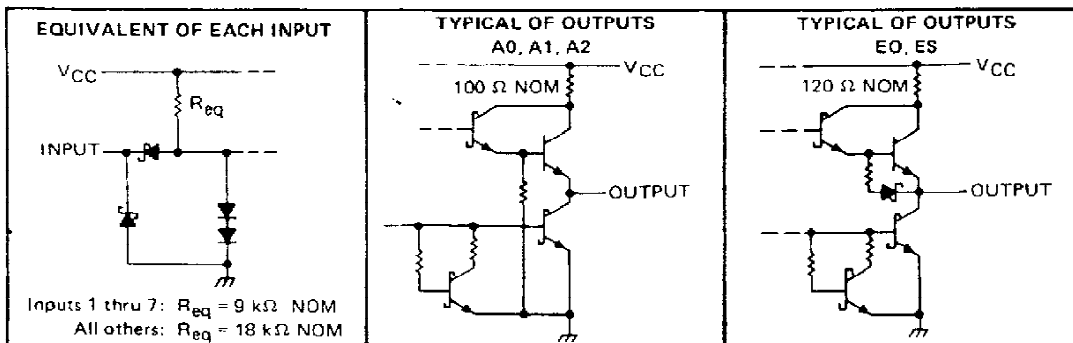
EQUIVALENT OF EACH INPUT	TYPICAL OF OUTPUTS A0, A1, A2	TYPICAL OF OUTPUTS EO, ES

Inputs 1 thru 7: R_{eq} = 9 kΩ NOM
All others: R_{eq} = 18 kΩ NOM

100 Ω NOM

120 Ω NOM

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage . . . . 7 V
Operating free-air temperature range: SN54LS348 . . . . −55°C to 125°C
 SN74LS348 . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS348 MIN	SN54LS348 NOM	SN54LS348 MAX	SN74LS348 MIN	SN74LS348 NOM	SN74LS348 MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	A0, A1, A2			−1			−2.6	mA
	EO, GS			−400			−400	μA
Low-level output current, I_{OL}	A0, A1, A2			12			24	mA
	EO, GS			4			8	mA
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		SN54LS348 MIN	SN54LS348 TYP[‡]	SN54LS348 MAX	SN74LS348 MIN	SN74LS348 TYP[‡]	SN74LS348 MAX	UNIT
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.7			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH} High-level output voltage	A0, A1, A2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OH} = −1 mA	2.4	3.1					V
			I_{OH} = −2.6 mA				2.4	3.1		
	EO, GS		I_{OH} = −400 μA	2.5	3.4		2.7	3.4		
V_{OL} Low-level Output voltage	A0, A1, A2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
	EO, GS		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
			I_{OL} = 8 mA					0.35	0.5	
I_{OZ} Off-State (high-impedance state) output current	A0, A1, A2	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.7 V			20			20	μA
			V_O = 0.4 V			−20			−20	
I_I Input current at maximum input voltage	Inputs 1 thru 7	V_{CC} = MAX, V_I = 7 V				0.2			0.2	mA
	All other inputs					0.1			0.1	
I_{IH} High-level input current	Inputs 1 thru 7	V_{CC} = MAX, V_I = 2.7 V				40			40	μA
	All other inputs					20			20	
I_{IL} Low-level input current	Inputs 1 thru 7	V_{CC} = MAX, V_I = 0.4 V				−0.8			−0.8	mA
	All other inputs					−0.4			−0.4	
I_{OS} Short-circuit output current[§]	Outputs A0, A1, A2	V_{CC} = MAX		−30		−130	−30		−130	mA
	Outputs EO, GS			−20		−100	−20		−100	
I_{CC} Supply current		V_{CC} = MAX, See Note 2	Condition 1		13	25		13	25	mA
			Condition 2		12	23		12	23	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§] Not more than one output should be shorted at a time.

NOTE 2: I_{CC} (condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open. I_{CC} (condition 2) is measured with all inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER[†]	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	1 thru 7	A0, A1, or A2	In-phase output	C_L = 45 pF, R_L = 667 Ω, See Note 3		11	17	ns
t_{PHL}						20	30	
t_{PLH}	1 thru 7	A0, A1, or A2	Out-of-phase output			23	35	ns
t_{PHL}						23	35	
t_{PZH}	EI	A0, A1, or A2				25	39	ns
t_{PZL}						24	41	
t_{PLH}	0 thru 7	EO	Out-of-phase output	C_L = 15 pF, R_L = 2 kΩ, See Note 3		11	18	ns
t_{PHL}						26	40	
t_{PLH}	0 thru 7	GS	In-phase output			38	55	ns
t_{PHL}						9	21	
t_{PLH}	EI	GS	In-phase output			11	17	ns
t_{PHL}						14	36	
t_{PLH}	EI	EO	In-phase output			17	26	ns
t_{PHL}						25	40	
t_{PHZ}	EI	A0, A1, or A2		C_L = 5 pF, R_L = 667 Ω		18	27	ns
t_{PLZ}						23	35	

[†] t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.
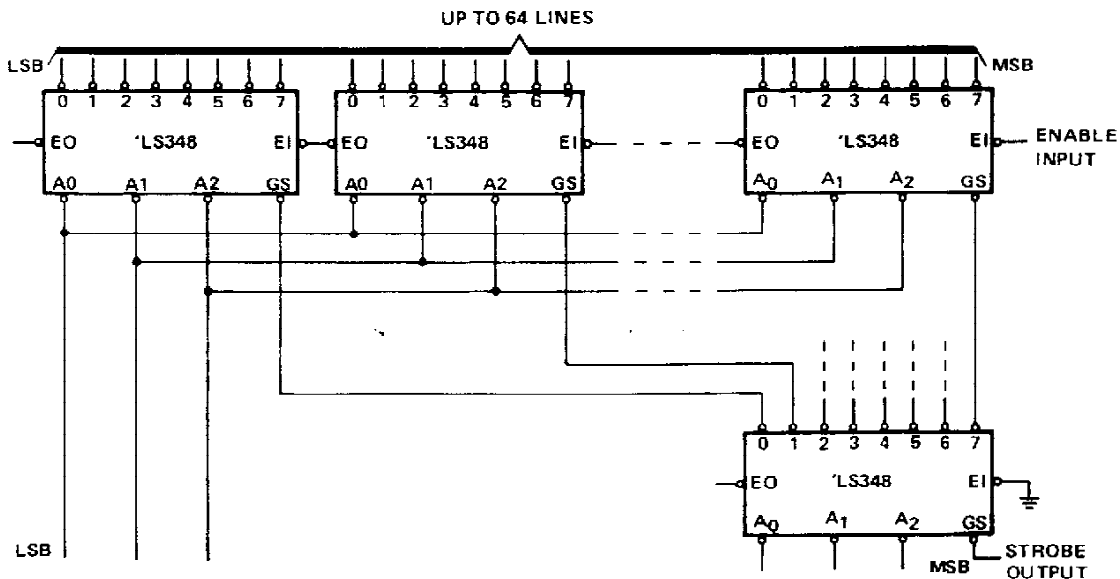

TYPICAL APPLICATION DATA

FIGURE 1—PRIORITY ENCODER WITH UP TO 64 INPUTS.

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