

CMOS Dual 2-Input NAND Buffer/Driver

High-Voltage Type (20-Volt Rating)

■ CD40107B is a dual 2-input NAND buffer/driver containing two independent 2-input NAND buffers with open-drain single n-channel transistor outputs. This device features a wired-OR capability and high output sink current capability (136 mA typ. at $V_{DD} = 10\text{ V}$, $V_{DS} = 1\text{ V}$). The CD40107B is supplied in the 8-lead dual-in-line plastic (Mini-DIP) package (E suffix), 14-lead hermetic frit-seal ceramic package (F suffix), and in chip form (H suffix).

Features:

- 32 times standard B-Series output current drive sinking capability — 136 mA typ. @ $V_{DD} = 10\text{ V}$, $V_{DS} = 1\text{ V}$
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin, full package temperature range, R_L to $V_{DD} = 10\text{ k}\Omega$:
1 V at $V_{DD} = 5\text{ V}$
2 V at $V_{DD} = 10\text{ V}$
2.5 V at $V_{DD} = 15\text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

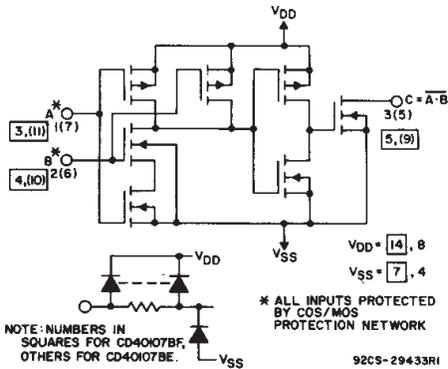
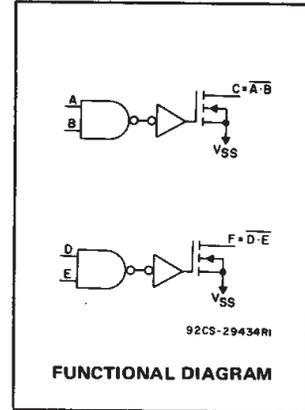


Fig.1 — Schematic diagram of CD40107B (one of 2 gates)

TRUTH TABLE

A	B	C
0	0	1*
1	0	1*
0	1	1*
1	1	0

*Requires external pull-up resistor (R_L) to V_{DD} .

#Without pull-up resistor. (3-state).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) -0.5V to +20V
Voltages referenced to V_{SS} Terminal	
INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to $V_{DD} + 0.5\text{V}$
DC INPUT CURRENT, ANY ONE INPUT $\pm 10\text{ mA}$
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW
OPERATING-TEMPERATURE RANGE (T_A) -55°C to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max $+265^\circ\text{C}$

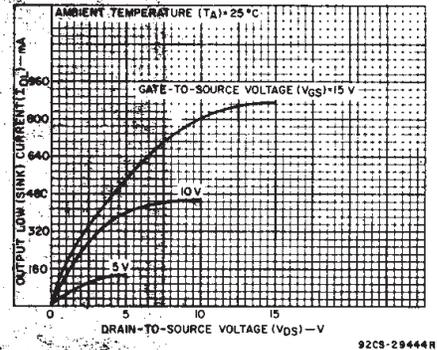


Fig.2 — Typical output low (sink) current characteristics.

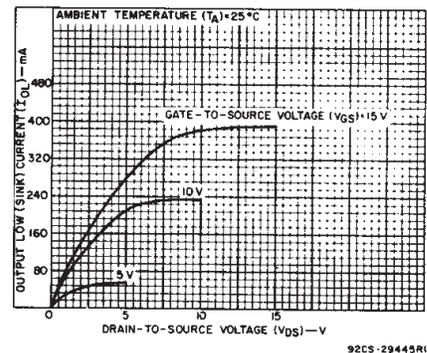


Fig.3 — Minimum output low (sink) current characteristics.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A = \text{Full Package-Temperature Range}$)	3	18	V

CD40107B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, Input $t_r, t_f = 20\text{ ns}$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		VDD Volts	Typ.	Max.	
Propagation Delay: High-to-Low, t_{pHL}	$R_L^* = 120\ \Omega$	5	100	200	ns
		10	45	90	
		15	30	60	
Low-to-High, t_{pLH}	$R_L^* = 120\ \Omega$	5	100	200	ns
		10	60	120	
		15	50	100	
Transition Time: High-to-Low, $t_{\tau HL}$	$R_L^* = 120\ \Omega$	5	50	100	ns
		10	20	40	
		15	10	20	
Low-to-High, $t_{\tau LH}$	$R_L^* = 120\ \Omega$	5	50	100	ns
		10	35	70	
		15	25	50	
Average Input Capacitance, C_{iN}	Any Input		5	7.5	pF
Average Output Capacitance, C_{oUT}	Any Output		30	—	pF

* R_L is external pull-up resistor to V_{DD} .

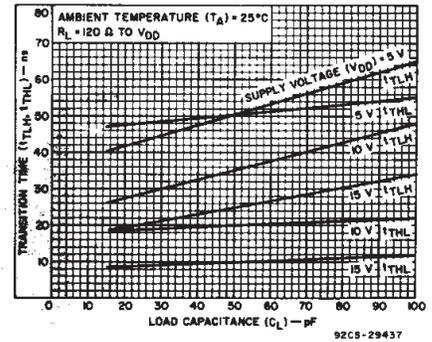


Fig. 4 — Typical transition time as a function of load capacitance.

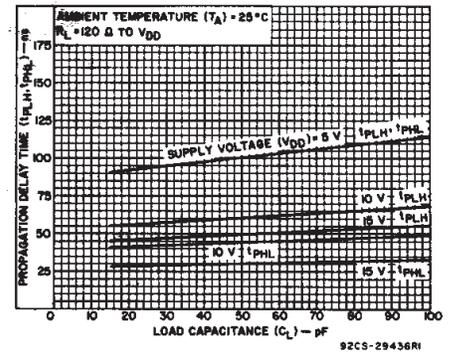


Fig. 5 — Typical propagation delay time as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES ($^\circ\text{C}$)							UNITS
				+25							
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current I_{DD} Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA
	—	0,10	10	2	2	60	60	—	0.02	2	
	—	0,15	15	4	4	120	120	—	0.02	4	
	—	0,20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0,4	0,5	5	21	20	14	12	16	32	—	mA
	1	0,5	5	44	42	30	25	34	68	—	
	0,5	0,10	10	49	46	32	28	37	74	—	
	1	0,10	10	89	85	60	51	68	136	—	
Output High (Source) Current I_{OH} Min.	No Internal Pull-Up Device										
Input Low Voltage V_{IL} Max.*	4,5	—	5	1,5			—	—	1,5	V	
	9	—	10	3			—	—	3		
	13,5	—	15	4			—	—	4		
Input High Voltage V_{IH} Min.*	0,5,4,5	—	5	3,5			3,5	—	—	V	
	1,9	—	10	7			7	—	—		
	1,5,13,5	—	15	11			11	—	—		
Input Current I_{IN} Max.	—	0,18	18	$\pm 0,1$	$\pm 0,1$	± 1	± 1	—	$\pm 10^{-5}$	$\pm 0,1$	μA
Output Leakage Current I_{OZ} Max.	18	0,18	18	2	2	20	20	—	10^{-4}	2	μA

* Measured with external pull-up resistor, $R_L = 10\text{ k}\Omega$ to V_{DD} .

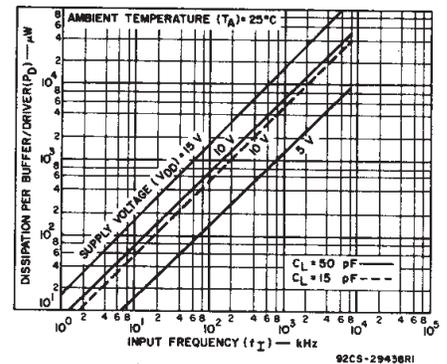


Fig. 6 — Typical power dissipation as a function of input frequency.

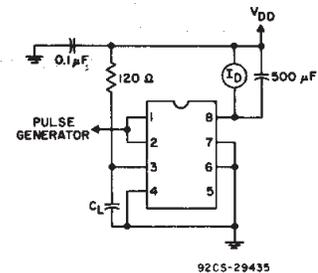
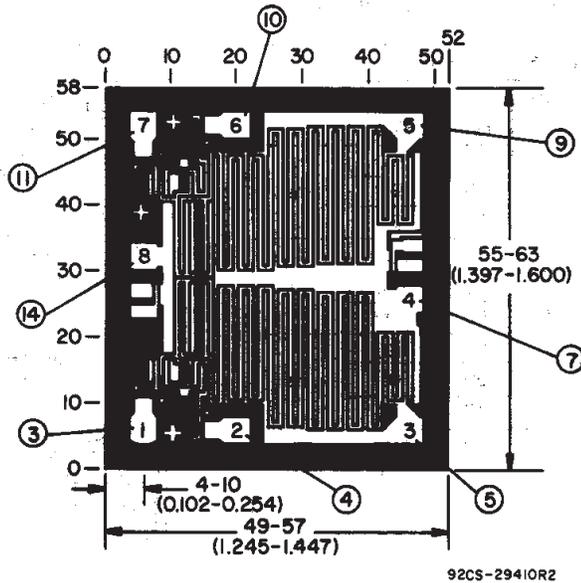


Fig. 7 — Power-dissipation test circuit for CD40107BE.

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HIGH VOLTAGE ICs

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Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

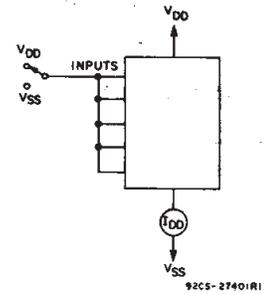


Fig. 8 - Quiescent-device current test circuit.

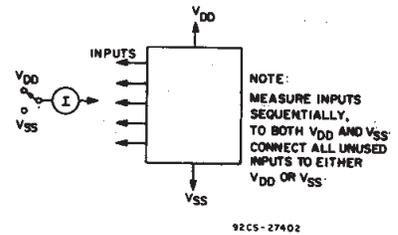
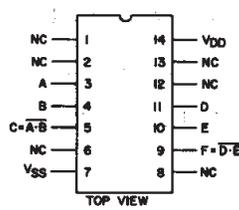
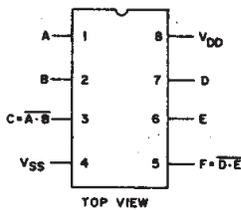


Fig. 9 - Input-current test circuit.



TERMINAL ASSIGNMENTS

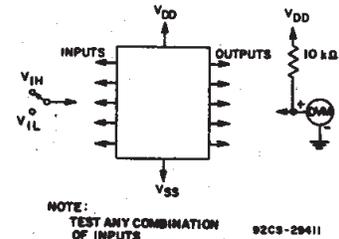


Fig. 10 - Input-voltage test circuit.

Special Considerations for CD40107B

1. Limiting Capacitive Currents for $C_L > 500$ pF, $V_{DD} > 15$ V.

For $V_{DD} > 15$ V, and load capacitance (C_L) from output to ground > 500 pF, an external 25Ω series limiting resistor should be inserted between the output terminal and C_L . No external resistor is necessary if $C_L < 500$ pF or $V_{DD} < 15$ V.

2. Driving Inductive Loads

When using the CD40107B to drive inductive loads, the load should be shunted with a diode to prevent high voltages from developing across the CD40107B output.

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